B.Sc. (H) Electronics : Semester III

Lecture Plan: Digital Electronics and Verilog

Date	Unit	Content
20-23 July'16	Unit 1	Number systems, Base conversions
25-30 July'16		Binary, Octal & Hexadecimal arithmatic, BCD code
01-06 Aug'16		Logic gates, Universal gate representations, Boolean algebra & theorems
08-13 Aug'16	Unit 2	Standard representation of logic gates (SOP & POS), K map minimization
15-20 Aug'16		Encoder-decoder, Multiplexer-demultiplexer, Implementing logic using multiplexers
22-27 Aug'16		Binary adder & subtractor, Parallel adder & subtractor, Flip flops
29 Aug'16 -03 Sep'16	Unit 3	Clocked and edge triggered flip flops, **Test 1**
05-10 Sep'16		Sequential Logic, State table, State Diagrams, Excitation table, Shift Registers
12-17 Sep'16		Counters: Synchronous, Asynchronous, Ring, Modulus N
19-24 Sep'16	Unit 1	Logic Families
26-30 Sep'16	Unit 4	**Test 2**, Programmable Logic devices
03-08 Oct'16		Introduction to Verilog, Structure of HDL module, Simulation and synthesis tools, Test Benches, Design: Data flow style, Behavioral style, Structural style
17-22 Oct'16		Language elements, Keywords, Identifiers, Logic values, Data types, Register types, Expressions
24-29 Oct'16		**Test 3**, Introduction to Gate level modelling, Built in primitive gates,
31 Oct'16 -05 Nov'16		MOS switches, bi-directional switches, Designing combinational and sequential circuits.
07-12 Nov'16		Revision